

LATCHED SENSE AMPLIFIERS AS HIGH SPEED
MEMORY IN A MEMORY SYSTEM

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ABSTRACT

A fault-tolerant, high-speed wafer scale system comprises a plurality of functional modules, a parallel hierarchical bus which is fault-tolerant to defects in an interconnect network, and one or more bus masters. This bus includes a plurality of bus lines segmented into sections and linked together by programmable bus switches and bus transceivers or repeaters in an interconnect network. By: 1) use of small block size (5 12K bit) for the memory modules; 2) use of programmable identification register to facilitate dynamic address mapping and relatively easy incorporation of global redundancy; 3) Use of a grid structure for the bus to provide global redundancy for the interconnect network; 4) Use of a relatively narrow bus consisting of 13 signal lines to keep the total area occupied by the bus small; 5) Use of segmented bus lines connected by programmable switches and programmable bus transceivers to facilitate easy isolation of bus defects; 6) Use of special circuit for bus transceivers and asynchronous handshakes to facilitate dynamic bus configuration; 7) Use of programmable control register to facilitate run-time bus reconfiguration; 8) Use of spare bus lines to provide local redundancy for the bus; and 9) Use of spare rows and columns in the memory module to provide local redundancy, high defect tolerance in the hierarchical bus is obtained.